REMARKS

In response to the Office Action dated November 7, 2000, the abstract and claims 1 and 3 are amended, and new claim 4 is added. Formal drawings will be submitted upon allowance of this application. Care has been exercised to avoid the introduction of any new matter.

Claims 1-3 have been rejected in the Office Action under 35 USC 112, second paragraph. Specifically, the Examiner states that it is not clear whether "the continuous grinding of the second step is done in the presence of the fixed abrasive grains from the first step" and whether "the grinding takes place continuously from the first step to the second step, or whether the continuous grinding takes place only within each step" (claim 1). With respect to claim 3, the Examiner sites the term "both" as being unclear. Applicants respectfully traverse the rejection with respect to claims 1 and 2, and amends claim 3.

Applicants respectfully direct the Examiner's attention to the first full paragraph on page 6 of the instant specification. This paragraph of the specification clearly indicates that after continuing rough grinding for a predetermined time, both sides of the semiconductor wafer 3 are continuously finish ground on the same grinding axis. With respect to claim 3, it has been amended to clarify that grinding occurs on both sides of the wafer.

Claims 1-3 have been rejected in the Office Action under 35 USC 102(b) as anticipated by Hasegawa (EP 0 745 456). Hasegawa discloses a method and apparatus for mirror-polishing a peripheral portion of a wafer. Figure 2 illustrates an apparatus 1 for mirror-polishing including a first polishing section 2 which carries out tape-polishing to the peripheral portion of the wafer and a second polishing section 3 which carries out buff-polishing to the peripheral portion.

Wafer device 11 includes a rotary body 11a which is driven by a motor to rotate around a vertical central axis, and four arms 11b. An absorption disc 11c, for holding a wafer on the lower surface, is provided on the lower portion of the top end of each arm 11b, as shown in Figure 6. A notch polishing device 12 includes a rotary drum 30a and a tape supporting member 30b. Inside the rotary drum 30a, there is tape T which comprises a tape base member and very fine abrasive grains. A portion of tape T in the notch polishing device 12 is pressed against the notch portion N of the wafer W and polishes the wafer W using tape T. Each of the orientation flat polishing device 13 and periphery polishing device 14 have a structure similar to notch polishing device 12.

The buff-polishing section 2 (i.e. the second polishing section) includes a second wafer positioning part G, a second notch polishing part H, an second orientation flat polishing part I and a periphery polishing part J. A second notch polishing device 22, a second orientation flat polishing device 23 and a second periphery polishing device 24 are also provided. The second notch polishing device 22 comprises a disc-shaped buff 22a made of a foam resin. The periphery of the rotating buff 22a is entered into the notch of the wafer W and is pressed against the notch portion N, while supplying an abrasive material comprising an aqueous solution containing a fine powder to the contacting surface of the buff. According to Hasegawa, because tape-polishing provided at a greater speed than that of buff-polishing is provided before polishing the peripheral portion of the wafer W by using a buff, the polishing time necessary to obtain a mirror-polished surface with a predetermined smoothness is shortened.

The present invention provides a method for grinding a semiconductor. Figure 1 illustrates a grinder that includes a pair of top and bottom grindstones 1, 2 arranged on the same line. The grindstones 1, 2 serve as fixed grindstones rotating in the same direction or opposite

directions at a high speed, and are fed in the axial direction. A semiconductor wafer 3 serves as a workpiece held between the grindstones 1, 2 at a position eccentric to the rotation center of the grindstones 1, 2, and rotates at a low speed. Hence, both sides of the wafer 3 can be ground by fixed abrasive grains. In this regard, the wafer 3 is place between grindstones 1, 2 at a low speed while driving the grindstones at a predetermined rotational speed and feed rate. After continuing rough grinding for a predetermined amount of time, both sides of the wafer 3 are continuously rough ground for a predetermined amount of time. The grinding occurs on the same grinding axis by continuing rotation of the grindstones 1, 2 and the wafer 3 while supplying a slurry which suspends fine abrasive grain between the grindstones 1, 2 from the slurry pipes 4 and 5. Significantly, both sides of the wafer 3 are efficiently ground up to a necessary accuracy before polishing without changing grindstones or using a lapping machine at the same time.

Applicants respectfully traverse the rejection. The claimed invention grinds a semiconductor wafer using fixed abrasive grains, and then continuously (i.e. seamlessly) grinds the wafer using free abrasive grains on the same grinding axis. That is, the wafer does not have to be removed from the grinding axis in between grinding using fixed abrasive grains and grinding using free abrasive grains. The applied reference, on the other hand, uses separate grinding axis for first and second polishing steps. Specifically, the applied reference carries out a first polishing step (2, 12, 13, 14) for polishing the peripheral portion of the wafer W by using tape T having abrasive grains thereon, and then a second polishing step to polish the peripheral portion of the wafer W by using a buff (22, 23, 24) with an abrasive material. To emphasize this distinction, claim 1 is amended to recite "grinding occurs on the same grinding axis".

Additionally, Hasegawa relates to a mirror polishing device, whereas the present invention relates to grinding which is accomplished before polishing. In this regard, a

semiconductor wafer is manufactured through the processes of grinding and polishing. Hence, it is readily understood that the processes of Hasegawa and the present invention differ fundamentally from one another.

Since the recited structure is not disclosed by the applied prior art, claim 1 is believed to be patentable. Claims 2-4, depending from claim 1, are similarly believed patentable. In view of the foregoing, claim 1-4 are believed to be in condition for allowance. An indication of the same is earnestly solicited.

Attached hereto is a marked up version of the changes made to the claims by the current amendment. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 47408200700 However, the Assistant Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A semiconductor wafer grinding method, comprising:

grinding a semiconductor wafer by fixed abrasive grains; and

continuously grinding the semiconductor wafer by free abrasive grains wherein grinding occurs on the same grinding axis.

3. (Amended) The semiconductor wafer grinding method according to claim 1, wherein grinding includes [both side] both sides of a semiconductor wafer or grinding of a chamfered portion.

4. (New) The semiconductor wafer grinding method according to claim 2, wherein grinding includes both sides of a semiconductor wafer or grinding of a chamfered portion.